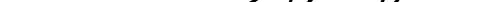


FOREIGN PATENT DOCUMENTS						
Exam. Initial ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
W	BA	0 397 994 A2		International Business Machines Corporation	11/22/1990	

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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 042P8931C	Application Number: 10/620,629	
Sheet 2 of 4		First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.	
		Filing Date: July 15, 2003	Art Unit: 2188	
OTHER ART - NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published		Translation ²
KN	A08	AGARWAL, A., et al., "The MIT Alewife Machine: A Large-Scale Distributed-memory Multiprocessor," <i>Technical Report MIT/LCS Memo TM-454, Laboratory for Computer Science, Massachusetts Institute of Technology</i> , 1991.		
KN	A19	ANDERSON, C., et al., "A Multi-Level Hierarchical Cache Coherence Protocol for Multiprocessors," <i>University of Washington</i> , 1992, 92-10-04		
KN	A18	ANDERSON, C., et al., "Design and Evaluation of a Subblock Cache Coherence Protocol for Bus-Based Multiprocessors," <i>University of Washington</i> , 1994, 94-05-02		
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KN	A20	CHAIKEN, D., et al., "LimitLESS Directories: A Scalable Cache Coherence Scheme," <i>Proceedings of the 4th Int'l Conference on ASPLOS</i> , pages 224-234, New York, April 1991.		
KN	A22	EGGERS, S.J., et al., "A Characterization of Sharing in Parallel Programs and Its Application to Coherency Protocol Evaluation," <i>Proceedings of the 15th Annual International Symposium on Computer Architecture</i> , May 1988.		
KN	A10	FARKAS, K., "Cache Consistency in Hierarchical-ring-based Multiprocessors," <i>Technical Report CSRI-273, Computer Systems Research Institute, University of Toronto</i> , Ontario, Canada, January 1993.		
KN	A11	FLEISCH, B., "A Coherent Distributed Shared Memory Design," <i>Proceedings from the 14th ACM Symposium on Operating System Principles</i> , pages 211-223, New York, 1989.		

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Sheet 3 of 4		First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
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OTHER ART - NON PATENT LITERATURE DOCUMENTS

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KN	A06	GHARACHORLOO, K., et al., "Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors," <i>Proceedings of the 17th International Symposium on Computer Architecture</i> , pages 15-26, May 1990.	
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KN	A23	LENOSKI, D., et al., "The Directory-based Cache Coherence Protocol for the Dash Multiprocessor," <i>Proceedings of the 17th Int'l Symposium on Computer Architecture</i> , Los Alamitos, Calif., May 1990.	
KN	A13	LI, K., et al., "Memory Coherence in Shared Virtual Memory Systems," <i>ACM Transactions On Computer Systems</i> , 7(4):321-359, November 1989.	
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Examiner Signature	<i>Keor Verbrugge</i>	Date Considered	8/19/05
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Sheet 4 of 4		First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
		Filing Date: July 15, 2003	Art Unit: 2188

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ICW	A24	NITZBERG, B., et al., "Distributed Shared Memory: A Survey of Issues and Algorithms," <i>IEEE Computer</i> , pages 52-60, August 1991.	
KW	A02	PAPAMARCOS, M., et al., "A Low-Overhead Coherence Solution for Multiprocessors with Private Cache Memories," <i>Proc. 11th ISCA</i> , 1984, pp. 348-354.	
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ICW	C01	Patent Act 1977: Examination Report under section 18(3), Application No: GB0309110.5 (International App. No. PCT/US01/30359), July 7, 2004	

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